



# UNITED STATES PATENT AND TRADEMARK OFFICE

*cler*

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,257	10/30/2003	William W. Cheng	03T004	2940
7590 David T. Yang, Esq. Morrison & Foerster LLP Suite 3500 555 est Fifth Street Los Angeles, CA 90013-1024		03/19/2007	EXAMINER WELLS, KENNETH B	
			ART UNIT 2816	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
2 MONTHS		03/19/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

Application Number: 10/698,257  
Filing Date: October 30, 2003  
Appellant(s): CHENG ET AL.

**MAILED**

**MAR 19 2007**

**GROUP 2800**

\_\_\_\_\_  
David T. Yang  
For Appellant

**EXAMINER'S ANSWER**

1. This is in response to the appeal brief filed on 1/19/07 appealing from the Office action mailed on 8/29/06.

**Real Party in Interest**

2. A statement identifying by name the real party in interest is contained in the brief.

**Related Appeals and Interferences**

3. There are no related appeals, interferences, or judicial proceedings which will directly affect or be directly affected

Art Unit: 2816

by or have a bearing on the Board's decision in the pending appeal.

#### **Status of Claims**

4. The statement of the status of claims contained in the brief is correct.

#### **Status of Amendments After Final**

5. The appellant's statement of the status of amendments after final rejection contained in the brief is correct

#### **Summary of Claimed Subject Matter**

6. The summary of claimed subject matter contained in the brief is correct.

#### **Claims Appendix**

7. The copy of the appealed claims contained in the Appendix to the brief is correct.

#### **Evidence Relied Upon**

6,333,672

Baskett

12-2001

AAPA Fig. 1

**Grounds of Rejection to be Reviewed on Appeal**

8. Claims 28, 29, 33, 35 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art Fig. 1 in view of Baskett.

As noted in the final rejection, applicant's admitted prior art (AAPA) Fig. 1 shows all of the limitations of the claims except for the recited cascode transistors and the second/third current sources. The recited first and second current summing buses in AAPA Fig. 1 are signal lines 16 and 18, respectively; the recited plurality of current switches are circuits 12 and 14, respectively; the recited first current sources (one within each current switch) are circuits 20 and 22; and the recited differential pairs of transistors are Q1/Q2 and Q3/Q4.

The recited cascode transistors and the second/third current sources (BJTs QA through QD in applicant's invention), though not disclosed, nevertheless would have been obvious to a person having ordinary skill in the art because the use of a pair of cascode transistors together with second/third current sources for providing respective "trickle" currents to the emitters of the cascode transistors is old and well-known in the art, one example being shown in Fig. 1 of Baskett. As seen in this figure, a pair of cascode BJTs 12, 14 are provided along with second and third current sources 16, 18 for providing

Art Unit: 2816

respective "trickle" currents to the emitters of the cascode transistors in the same manner as those of applicant's invention (i.e., BJTs QA through QD in instant Fig. 3). Baskett describes his trickle current sources as "keep alive" current sources, see column 1, lines 41-61, where these current sources 16, 18 (and also the cascode BJTs) are added to a conventional differential amplifier in order to achieve several specific benefits/advantages (i.e., reducing miller capacitance, reducing switching delays, and reducing voltage variations at the output nodes). As to the limitation that the trickle currents are approximately 10 to 100 times smaller than the current flowing through the first current source, note the discussion in Baskett that his keep alive current sources 16, 18 are made so small that the currents through BJTs 12 and 14 will only be a "nominal" amount of current even when the differential transistors 20/22 are off (column 1, lines 52-55).

As to the use of a driver circuit in claim 37, having the structure/function recited in claims 38 and 39, see the rejection set forth in paragraph seven of the office action mailed on 11/16/04 where such a driver circuit limitation was rejected as being obvious as well.

### Response to Arguments

9. Appellant makes various arguments throughout the brief, but none of these arguments is persuasive, as detailed below.

The first argument is that "the admitted prior art, even when combined with Baskett, do not contain any disclosure or suggestion of the DAC recited in Claim 28." This argument is not persuasive because AAPA Fig. 1 clearly shows a DAC, and when that DAC is combined with the teachings of Baskett Fig. 1, all of the limitations set forth in independent claim 28 will be met under 35 U.S.C. 103.

The second argument is that neither AAPA Fig. 1 nor Baskett Fig. 1 discloses that the trickle currents are approximately 10 to 100 times smaller than the current flowing through the first current source. This argument is not persuasive for two reasons. First, the recitation of "approximately 10 to 100 times smaller" leaves open the possibility that the trickle current level can be outside of the range "10 to 100 times smaller." Second, and more importantly, Baskett specifically indicates that his keep alive (trickle) current sources 16, 18 are made so small that the current through BJTs 12 and 14 will only be a "nominal" amount of current even when the differential transistors 20 and 22 are off (column 1, lines 52-55). This disclosure by Baskett would be understood by individuals having

Art Unit: 2816

ordinary skill in the art that, when BJT 20 is off, in order to keep a nominal amount of current flowing through BJT 12, it is essential that the current flowing through BJT 16 also be only a nominal amount (without BJT 16, no current would flow through BJT 12 when transistor 20 is off, whereas with a small BJT 16, a nominal current will flow through the path from VCC to ground through transistors 12 and 16). The same conditions will apply for the current path from VCC to ground through transistors 14 and 18. Moreover, as set forth by the CCPA in *In re Aller*, 105 USPQ 233 (1955), "where general conditions of a claim are disclosed by the prior art, it is not inventive to discover optimum or workable ranges by routine experimentation." Stated differently, the particular range recited in the claims is not seen to be critical and the claimed range is "within the capabilities" of persons having ordinary skill in the art of semiconductor integrated circuits.

The third argument is that "the Examiner did not satisfy his burden of showing motivation to combine Baskett with Fig. 1 of the present application." This argument is not persuasive because the motivation is clearly set forth in the office action, i.e., to achieve the benefits/advantages described by Baskett that are achieved when cascode and trickle current sources are used in a conventional BJT differential amplifier.

The fourth argument is that Baskett uses cascode transistors and keep alive (i.e., trickle) current sources as part of a differential logic circuit and "it would be contrary to conventional wisdom of one skilled in the art, from a digital logic perspective as taught by Baskett, to construct an analog output circuit...by incorporating the pure digital circuitry shown in Fig. 1 of Baskett with that of DAC [sic] of Fig. 1 of the present application." This argument is similarly not persuasive. As one skilled in the art will easily recognize, the Baskett Fig. 1 circuit and the current steering cells 12, 14 are the same type of circuits, i.e., they all receive digital inputs (i.e., "1" or "0" bits), and in response thereto, a predetermined current flows out of either Q1 or Q2 in cell 12 (depending on which of Q1, Q2 is on) and a predetermined current also flows out of either Q3 or Q4 (depending on which of these BJTs is on) in cell 14. As the ordinarily skilled artisan also recognizes, the outputs flowing from the differential BJTs are either logic "1" or logic "0", e.g., when BJT Q1 is on, Q2 will be off, and vice-versa. When one of the BJTs Q1, Q2, Q3 and Q4 is on, that transistor outputs current from current source 20 or 22 and this current output represents a logic "1" state. When the BJT is off, it outputs no current, and thus its output is logic "0". This operation is the same in Baskett's Fig. 1

Art Unit: 2816

circuit (which is the reason Baskett refers to his Fig. 1 as a differential logic circuit) and also in appellant's current steering cells (also referred to in the instant specification as "current switches"). Thus, to argue that Fig. 1 of Baskett is a differential logic circuit whereas the present invention is a DAC, is not on point, i.e., the rejection is simply replacing the differential circuits 12 and 14 with the differential logic circuit of Baskett Fig. 1 (there is clear motivation to do so). As a person having ordinary skill in the art will recognize, Fig. 1 of Baskett and AAPA circuits 12 and 14 are all differential logic circuits, and thus to argue that they "serve fundamentally different purposes and operate in very different ways" is incorrect. They are in fact the same type of circuits, that of Baskett Fig. 1 simply being an improvement over AAPA Fig. 1 circuits 12 and 14 (due to the use of cascode and keep alive bipolar junction transistors by Baskett). The "analog" function/operation of AAPA Fig. 1 is achieved by the summing of the various digital outputs (i.e., logic "1" current flowing through each of BJTs Q1 through Q4 out to bus lines 16 and 18). While it is correct that the Baskett Fig. 1 circuit is a differential logic circuit and AAPA Fig. 1 shows a DAC, such does not mean there is no motivation to combine their teachings. The rejection is simply replacing the differential logic

Art Unit: 2816

circuits 12, 14 of AAPA Fig. 1 with the (improved) differential logic circuit shown in Baskett's Fig. 1.

The further arguments, that the combined prior art noted above does not meet the limitations of the buffer transistor (BJT Q5 in instant Fig. 3) or the driver circuit of claims 37-39, are also not persuasive. The recited buffer transistor reads on BJT Q5 or Q7 shown in instant Fig. 1 (and also reads on BJT 24 in Fig. 1 of Baskett, the "current source" of Baskett being the resistor at the emitter of this transistor). The recited driver circuit is shown in instant Fig. 2, as further admitted prior art. Note the rejection set forth in the 11/16/04 office action (paragraph seven thereof).

The next argument, that "the Primary Examiner did not point to any reasons *why* an ordinary artisan would have combined the references to construct the structure recited in Claim 28 of the present application (emphasis in original)", is again not persuasive because the motivation is clearly set forth in the office action and in Baskett (see the rejection above).

Appellant's final argument is that the examiner relied upon hindsight reconstruction in order to combine the teachings of AAPA and Fig. 1 of Baskett. This argument is also not persuasive because the motivation for combining the circuits of AAPA Fig. 1 and that of Baskett is clearly set forth in the

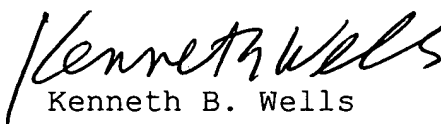
Art Unit: 2816

office actions and in Baskett, as noted above.

### Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



Kenneth B. Wells  
Primary Examiner  
Art Unit 2816

### Conferees:

Timothy P. Callahan, SPE Art Unit 2816

Darren E. Schuberg, SPE Art Unit 2834

